A 39 μW Body Channel Communication Wake-up Receiver with Injection-locking Ring-oscillator for Wireless Body Area Network

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***Abstract*— An ultra-low power wake-up receiver for body channel communication (BCC) is implemented in 0.13μm CMOS process. The proposed wake-up receiver uses the injection-locking ring-oscillator (ILRO) to replace the RF amplifier with low power consumption. Through the ILRO, the frequency modulated input signal is converted to the full swing rectangular signal which is directly demodulated by the following low power PLL based FSK demodulator. In addition, the relaxed sensitivity and selectivity requirement by the good channel quality of the BCC reduces the power consumption of the receiver. As a result, the proposed wake-up receiver achieves a sensitivity of -55.2dbm at a data rate of 200kbps while consuming only 39μW from the 0.7V supply.**

I. INTRODUCTION

Recently, wireless body-area-network (WBAN) is getting more attention due to the emerging applications to next-generation healthcare and entertainment [1]. The major design challenge associated with the WBAN is to extend the lifetime of the WBAN devices under limited energy source. Since one of the most power-consuming parts in the WBAN devices is the wireless transceiver, the body channel communication (BCC) which uses the human body as a communication channel is suggested for the low power wireless transceiver [2]-[4]. The BCC uses the low frequency band (30 – 120 MHz) and electrode rather than the low impedance antenna. Therefore, the BCC has been energy efficient solution for WBAN.

In the BCC as well as other communication method such as narrow band (NB) or ultra wide band (UWB) communication, the transceiver should be heavily duty-cycled in order to reduce the energy consumption. The usage of the wake-up receiver is possible solution for the efficient duty-cycled communication. Without the wake-up receiver, each transceiver periodically monitors the channel to listen for potential incoming wake-up signal, which increases the overall power consumption of the WBAN system and communication latency. The wake-up receiver continuously monitors the channel for requests and activates the transceiver. However, the power consumption of the wake-up receiver must be negligible compared to the main transceiver because it is always turned on. Since the power consumption of the BCC transceiver is lower than the RF transceiver, the BCC wake-up receiver should dissipate less active power than the previous state-of- the-art wake-up receiver [8]-[11].

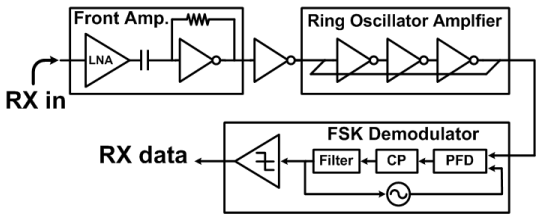

Figure 1. Overall architecture.

To satisfy the tight power budget, in this paper, we present an ultra-low power BCC wake-up receiver with injection-locking ring-oscillator (ILRO) for WBAN applications. Fig 1 shows the overall architecture of the proposed ILRO based wake-up receiver. By injection-locking to power-efficient ring oscillator, the weak input signal is converted to the full swing rectangular signal which is directly demodulated by the low power PLL-based FSK demodulator. The reason why the proposed BCC wake-up receiver is able to significantly reduce the power consumption is as follows. First, the low power ILRO is proposed to replace the high gain RF amplifier which consumes lots of power. Second, thanks to the superior channel quality of BCC, the sensitivity requirement of the wake-up receiver is mitigated. At last, the low frequency band of BCC (30 – 120 MHz) reduces the selectivity requirement of the receiver. Thanks to these features, the proposed BCC wake-up receiver consumes only 39μW with a sensitivity of -55.2dBm at a data rate of 200kb/s.

The rest of the paper is organized as follows. In Section II, the architecture of the proposed wake-up receiver will be explained with other low power wake-up receiver architecture. After Section III describes building blocks of the wake-up

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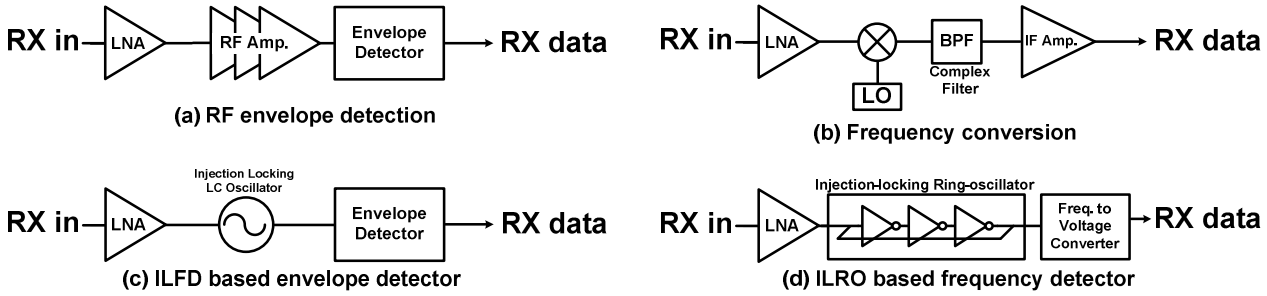


Figure 2. Comparison of receiver architectures. (a) Frequency conversion. (b) RF envelope detection. (c) ILFD based envelope detector. (d) ILRO based frequency architecture.

receiver, Section IV will show the implementation results. Finally, Section IV concludes the paper.

II. ARCHITECUTRE OVERVIEW

Fig 2 shows the previous and proposed architecture for the low power wake-up receiver. Fig 2 (a) is the envelope detection based architecture which is the energy-efficient way to implement the wake-up receiver [9]-[10]. It has simple architecture with just RF amplification and envelope detection. However, there are two drawbacks. First, the high RF gain is required due to overcome the nonlinear nature of the envelope detector. Second, the high Q-factor of the RF filter for the selectivity need external component such as BAW resonator. Consequently, the power consuming high RF gain without external components makes it difficult to adopt the envelope detection architecture for the wake-up receiver owing to the tight power budget and system cost.

The frequency conversion architecture down-converts the high frequency signal into low frequency signal as shown in Fig 2 (b). Since the gain amplification and the filtering are realized at a lower frequency, overall power consumption can be decreased without the need of high Q-factor filter. However, in this architecture, bulk of the power consumption is dedicated to the high accuracy local oscillator (LO). To implement the low power wake-up receiver without power-hungry LO, the uncertain-IF architecture is proposed in [8]. It reduces the power consumption significantly by replacing the high-accuracy LO to ring oscillator. However, this architecture should reject the image frequency by external component or power consuming complex filter.

Meanwhile, in the Fig 2 (c), the injection-locking frequency divider (ILFD) based architecture [5] is proposed to reduce the gain overhead of the RF amplifier which is the drawback of the envelope detection architecture. Since the gain requirement of the RF amplifier is determined by the locking range of the LC oscillator rather than nonlinear envelope detector, required RF gain and the power consumption are decreased. However, due to the frequency-to-amplitude conversion property, the power-hungry LC oscillator should be utilized, which increases the overall power consumption.

From these observations, for the low power wake-up receiver, the ILRO based architecture is proposed in Fig 2 (d). Through the ILRO, weak input signal is converted to the full swing rectangular signal with negligible power consumption. The output signal of ILRO is directly demodulated by the low power PLL-based FSK demodulator. In this architecture, ILRO replaces the high gain RF amplifier shown in Fig 2 (a) with the low power consumption. In addition, it doesn't need any external components or complex filter for down-conversion as shown in Fig 2 (b). Furthermore, to reduce the power consumed by LC oscillator in Fig 2 (c), the LC oscillator is replaced by power-efficient ring oscillator. The frequency-to-voltage converter is exploited to directly demodulate the output of the ILRO. As a result, the proposed ILRO based architecture has the advantages over the previous receiver architecture of the low power wake-up receiver.

III. BUILDING BLOCKS

The wake-up receiver uses the carrier frequency of 35MHz with a frequency deviation of 10MHz, which is the lowest frequency in BCC frequency band [4]. The 0.7V supply voltage is used to reduce the overall power consumption. The overall transceiver is composed of the front-end amplifier,

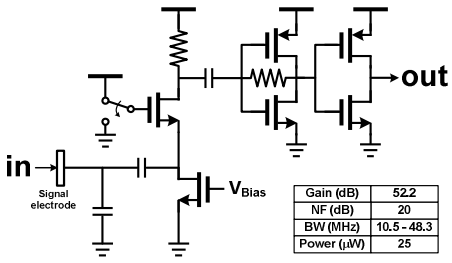


Figure. 3. Schematic of the front-end amplifier.

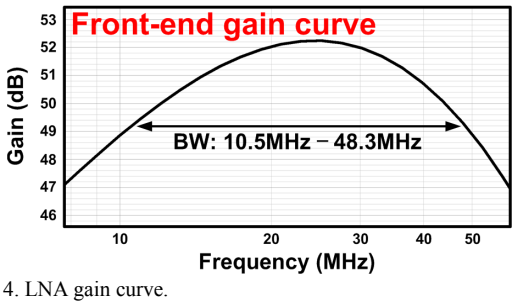


Figure. 4. LNA gain curve.

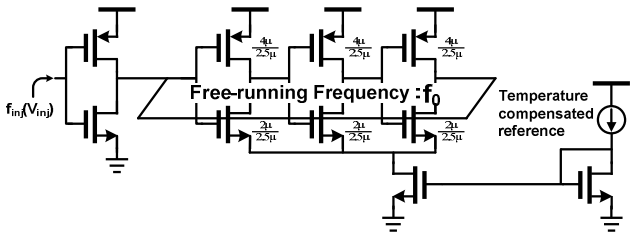


Figure. 5. Injection-locking ring-oscillator.

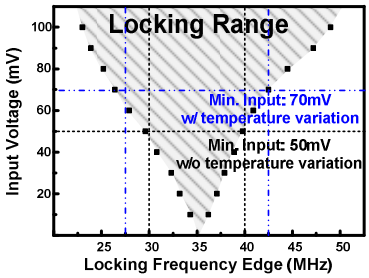


Figure. 6. Relationship with locking range and input amplitude.

ILRO, and PLL based demodulator.

A. *Front-end Amplifier*

Fig 3 is the schematic of the front-end amplifier. Since the sensitivity requirement is lower than the RF receiver by the good channel quality as mentioned in the introduction, the front-end amplifier focuses on obtaining the high voltage gain and low power consumption with mitigated noise requirement. The front-end amplifier consists of two stage amplifier. The first stage which interfaces with the signal electrode uses the common gate configuration to reduce the input impedance. The second stage amplifier is based on the resistive feedback inverter to achieve the high voltage gain with low power consumption. The effective-g_m of the amplifier is boosted by the current reuse scheme, which efficiently increases the voltage gain of the amplifier. Fig 4 is the gain curve of the front-end amplifier with 10.5-48.3MHz bandwidth. As a result, overall gain is 52dB with 20dB NF and power consumption is 25μW from the 0.7V supply voltage.

B. *Injection-locking Ring-oscillator*

Fig 5 describes the schematic of the ILRO. The ring oscillator is composed of three inverters with tail current source. In order to ensure the frequency stability of the ring oscillator, the temperature compensated current source is utilized. The frequency drift is within 2.5MHz over the 90°C temperature variation. In terms of [6] and [7], the locking range is proportional to the amplitude of the input signal. If the input amplitude is large, the locking range of the ring oscillator increases, and vice versa. Fig 6 shows the relationship between the input amplitude (V_{inj}) and the locking range of the ILRO. Since the frequency deviation is 10MHz, the amplitude of the input voltage should be larger than 50mV. On the other hand, considering the frequency drift of the ring oscillator, the input amplitude should be increased to ensure the locking range of 10MHz over the temperature variation. Because the frequency drift is within 2.5MHz by the temperature compensated reference, the input amplitude should be larger than 70mV to compensate the frequency drift of the ring oscillator if the free running frequency of the ring oscillator is tuned to 35MHz.

C. *PLL Based Demodulator*

The PLL-based demodulator is proposed to directly demodulate the full swing rectangular signal of the ILRO output (Fig. 7). Since the frequency deviation is relatively large compared to the carrier frequency, ring voltage-controlled oscillator (VCO) is used to build the high VCO gain with the low power consumption as shown in Fig. 8. The free running frequency is determined by I_{tail} and it is generated by the temperature-compensated reference circuit. In order to control the oscillation frequency, additional tail current I_{ctrl} is applied. The source resistor R_s increase the linearity of the VCO gain curve as shown in Fig. 9. The linear region is from 0.37V to 0.6V, and corresponding VCO gain is 60.2MHz/V. For the low power consumption, 10μA of the pumping current is used in charge pump. The loop bandwidth of 250kHz covers the data rate of 200kbps. The value of the R_1, C_1, and C_2 is 2.8kΩ, 840pF, and 65pF, respectively.

IV. Implementation Results

A. *Sensitivity analysis*

The sensitivity of the proposed wake-up receiver can be limited by two conditions. First condition is determined by the locking range of the ring-oscillator. The locking range of the ILRO determined by input power should cover the input frequency deviation. It means that the minimum input power of the receiver is limited by the required input power of the ILRO and the gain of the front-end amplifier as follows.

$$P_{min} = (ILRO\ minimum\ input)/(gain) \quad (1)$$

Following that equation, the input sensitivity limited by the locking range condition is achieved as -65.1dbm with the ILRO minimum input of 70mV and front-end gain of 52dB.

The second condition is considered by the signal-to-noise ratio (SNR) requirement of the receiver chain. The noise

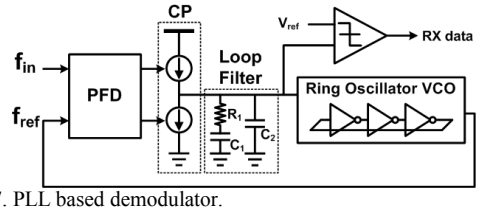


Figure. 7. PLL based demodulator.

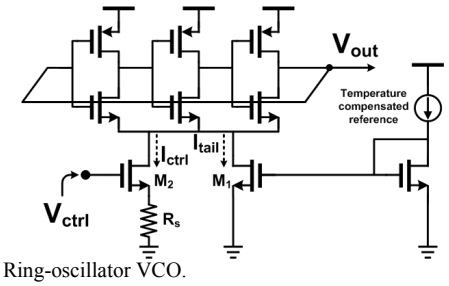


Figure. 8. Ring-oscillator VCO.

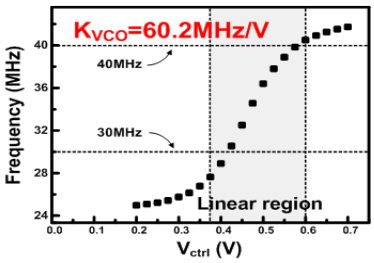


Figure. 9. VCO gain curve.

performance and bandwidth of the front-end amplifier with required minimum SNR has effect on the sensitivity through the following equation.

$$P_{min} = -174dBm + NF + 10\,log(BW) + SNR_{req} \quad (2)$$

With the NF of 20dB, bandwidth of 37.8MHz, and required SNR of 20dB which allows the BER less than 0.001% in the non-coherent FSK demodulator, the sensitivity is limited by -55.2dBm.

From the analysis, the sensitivity is estimated to -55.2dBm by (2). It should be noticed that at the input signal of -55.2dBm, the locking range of the ILRO is far larger than 10MHz, therefore, the frequency drift of the ring oscillator over the temperature variation has negligible effect on performance of the receiver without the additional frequency calibration.

B. Simulation results

The eye diagram of the demodulated bit streams at the input power of -50dBm is shown in Fig. 10. The 200kbps pseudo-random data is applied to obtain the eye diagram. Since the input power is large enough to cover frequency deviation of 10MHz, there is almost no jitter in the demodulated signal. The performance summary with layout diagram and the comparison with the previous works are listed in Fig. 11 and Table I. The proposed wake-up receiver

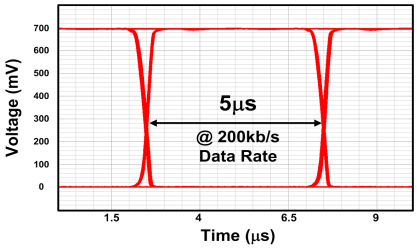
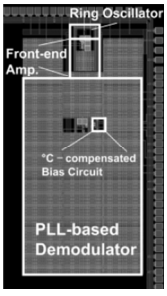


Figure. 10. The eye diagram of the receiver.



Modulation	FSK
Carrier Frequency	35MHz
Deviation	10MHz
Data Rate	200kbps
Supply Voltage	0.7V
Power	
Front-end Amp	25µW
Ring Oscillator	4µW
Demodulator	10µW
Total	39µW
Sensitivity	-55.2dBm
Area	2mm x 1mm
Process	0.13 µm

Figure. 11. Layout diagram and summary

Table. I. Comparison with previous wake-up receivers.

	This Work	[8]	[9]	[10]	[11]
Power (µW)	39	52	65	51	415
Sensitivity (dBm)	-55.2	-72	-48	-75	-82
Data Rate (kbps)	200	100	100	100	500
Energy Efficiency (pJ/bit)	195	520	650	510	830
External Components	X	BAW, XTAL	BAW	X	X
Process (nm)	130	90	90	90	65

with ILRO achieves the lowest power consumption among the reported state of the art wake-up receiver in our table without the help of the external components.

V. CONCLUSION

In this paper, ultra-low power BCC wake-up receiver is proposed for WBAN. The ILRO replaces the high gain RF amplifier with low power consumption. The weak input signal is converted to the full swing rectangular signal through ILRO and directly demodulated by the low power PLL-based demodulator. In addition, the relaxed sensitivity and selectivity requirement by the good channel quality of the BCC reduces the power consumption of the receiver. As a result, the proposed wake-up receiver implemented in 0.13µm CMOS technology consumes only 39µW with a sensitivity of -55.2dBm at a rate of 200kbps.

VI. ACKNOWLEDMENT

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